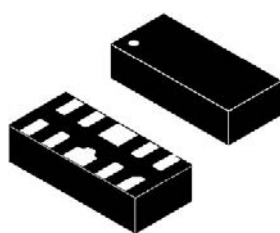


Ultra Low Capacitance Array for ESD Protection
FEATURES

- Ultra low capacitance: 0.33pF(typical) for each channel
- Up to four I/O lines of protection
- Low operating voltage: 3.3V
- Low leakage current: 0.1 μ A @ VRWM (typical)
- Low clamping voltage
- Protects four data lines
- Low operating and clamping voltage
- Meets MSL level 3

MECHANICAL DATA

- Case : Molded, plastic DFN-10
- Polarity : Shown follows
- Epoxy : UL94-V0 rated flame retardant

DFN-10 PACKAGE


Marking Code


Note:

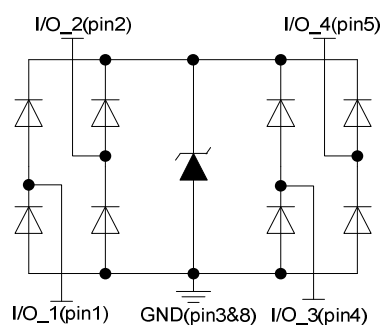
- (1) "Dg" is the part number of SEDFN03V4, fixed.
- (2) "Y" is year code, from 0 to 9, for 2015 "Y" is 5.
- (3) "W" is date code. "W" is the assembly week in a year, from 1 to 0, A to Z.
- (4) "A" is the production lot number, from A to Z.

APPLICATIONS

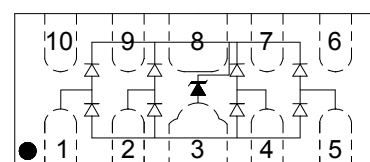
- Serial ATA
- PCI express
- Desktops, servers and notebooks
- MDDI ports
- USB2.0, 3.0 and 3.1
- Display ports
- HDMI 1.3, 1.4 and 2.0
- Digital visual interfaces (DVI)

IEC COMPATIBILITY

- IEC 61000-4-2 (ESD) ± 15 kV (air), ± 8 kV (contact)
- IEC 61000-4-4 (EFT) 40A (5/50ns)
- IEC 61000-4-5 (Lightning) 3A (8/20 μ s)

SCHEMATIC & PIN CONFIGURATION


Pin configuration



Top view

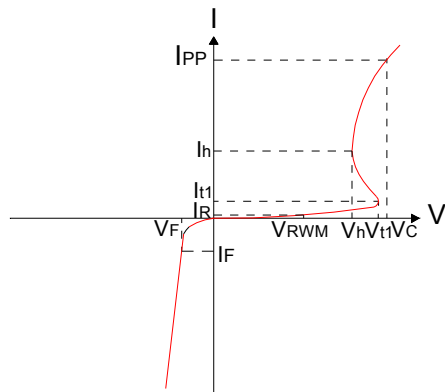
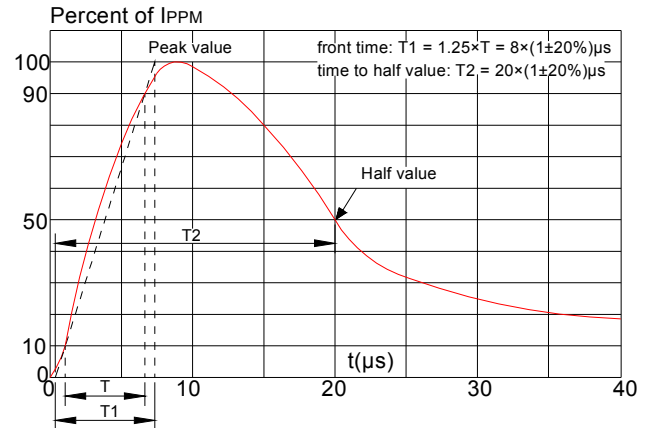
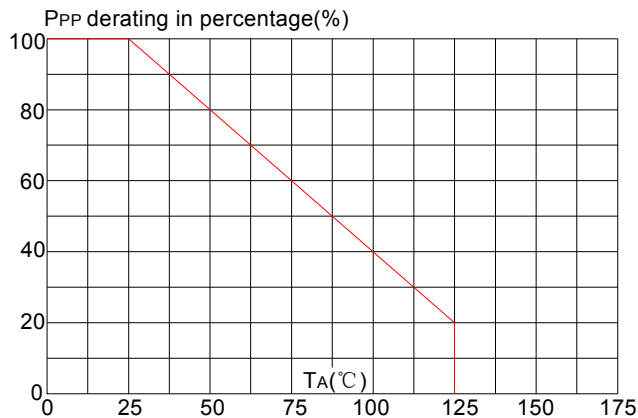
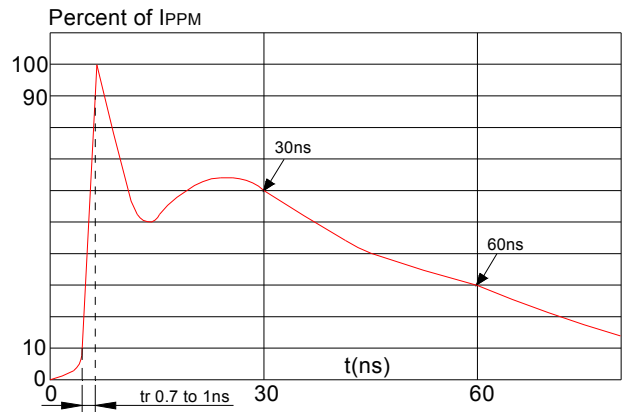
ABSOLUTE MAXIMUM RATINGS ($T_A=25^{\circ}\text{C}$, RH=45%-75%, unless otherwise noted)

Parameter	Symbol	Value	Unit
Peak pulse power dissipation on 8/20 μs waveform	P_{PP}	30	W
ESD per IEC 61000-4-2 (Air) ESD per IEC 61000-4-2 (Contact)	V_{ESD}	+/- 15 +/- 8	kV
Lead soldering temperature	T_L	260 (10 sec.)	$^{\circ}\text{C}$
Operating junction temperature range	T_J	-55 to +125	$^{\circ}\text{C}$
Storage temperature range	T_{STG}	-55 to +150	$^{\circ}\text{C}$

ELECTRICAL CHARACTERISTICS ($T_A=25^{\circ}\text{C}$)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Reverse working voltage	V_{RWM}	I/O to GND			3.3	V
Reverse leakage current	I_R	I/O to GND @ $V_{RWM}=3.3\text{V}$		0.1	1.0	μA
Reverse triggering voltage	V_{t1}	I/O to GND @ $I_{t1}=1\mu\text{A}$	3.8			V
Reverse holding voltage	V_h	I/O to GND @ $I_{h1}=1\text{mA}$		4.0	5.5	V
Clamping voltage	V_C	$I_{PP}=1\text{A}$, $t_P=8/20\mu\text{s}$		8	9	V
		$I_{PP}=3\text{A}$, $t_P=8/20\mu\text{s}$		10	11	
Junction capacitance	C_J	$V_{RWM}=3.3\text{V}$, $f=1\text{MHz}$ I/O pin to GND		0.33	0.39	pF
		$V_{RWM}=3.3\text{V}$, $f=1\text{MHz}$ Between I/O pins		0.2	0.3	pF

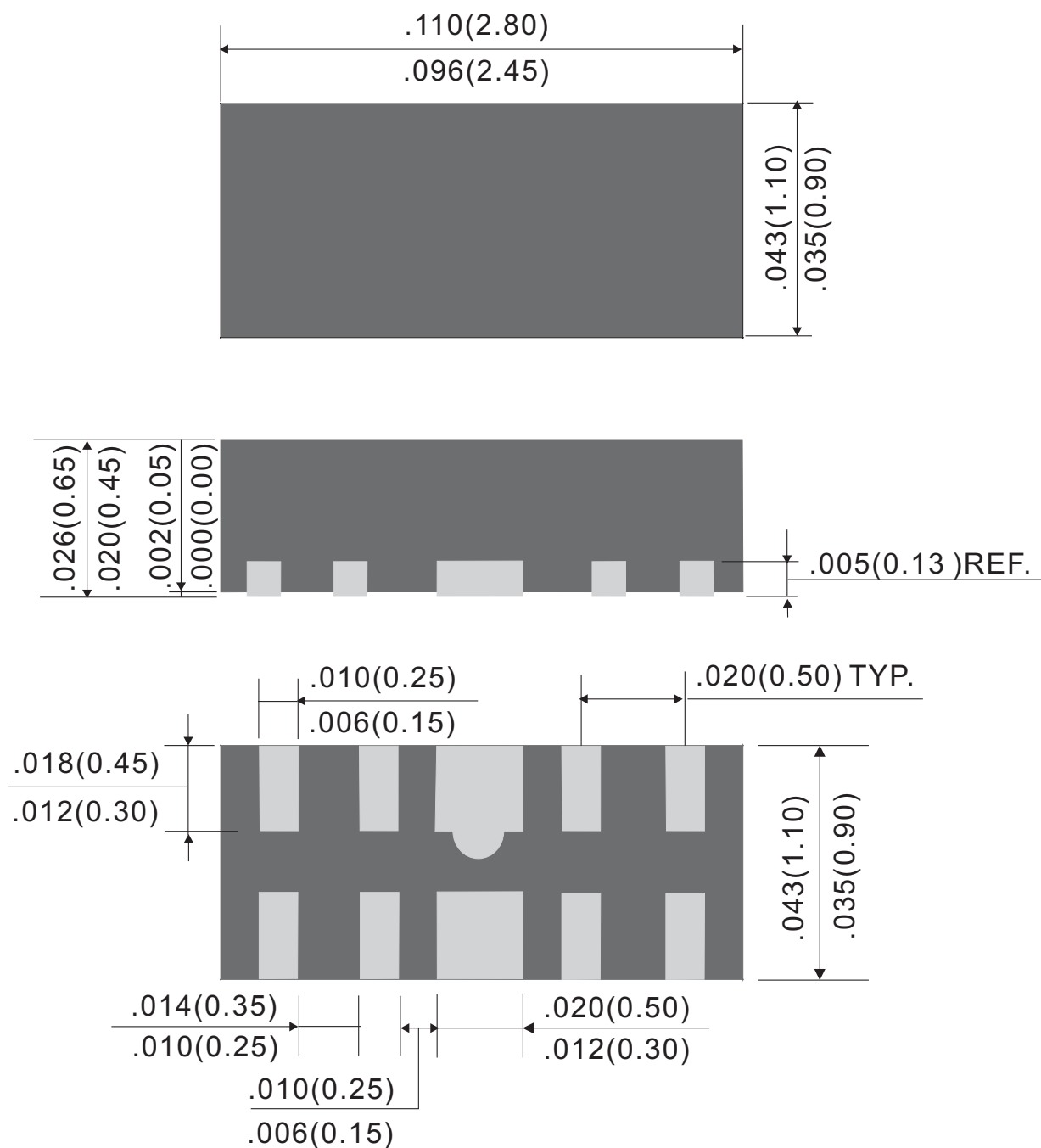
RATINGS AND V-I CHARACTERISTICS CURVES ($T_A=25^{\circ}\text{C}$, unless otherwise noted)

FIG.1: V- I curve characteristics (Uni-directional)

FIG.2: Pulse waveform (8/20 μs)

FIG.3: Pulse derating curve

FIG.4: ESD clamping (8KV contact)




Outline Drawing

DFN-10



Dimensions in inches and (millimeters)

Rev.G

Suggested Soldering Pad Layout	DFN-10
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The diagram illustrates the suggested soldering pad layout for a DFN-10 package. It features five yellow rectangular soldering pads arranged in a row. The dimensions are specified in inches and millimeters (in parentheses):

- Overall Width:** .061 (1.56)
- Pad Spacing (Pitch):** .039 (1.00)
- Pad Width:** .020 (0.5)
- Pad Height:** .027 (0.68)
- Distance from Pad Center to Pad Edge:** .008 (0.20)
- Distance from Pad Center to Pad Edge:** .015 (0.40)

Dimensions in inches and (millimeters)

RevA

Ordering Information:

Device PN	Packing
SEDFN03V4 -T ⁽¹⁾ H ⁽²⁾ -WS ⁽³⁾	Tape&Reel: 3 Kpcs/Reel

Note: (1) Packing code, Tape & Reel Packing

(2) Halogen free product for packing code suffix "H"

(3) WS : Willas brand abbreviation, Label Type does not display

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